FX803 Audio Signalling Processor

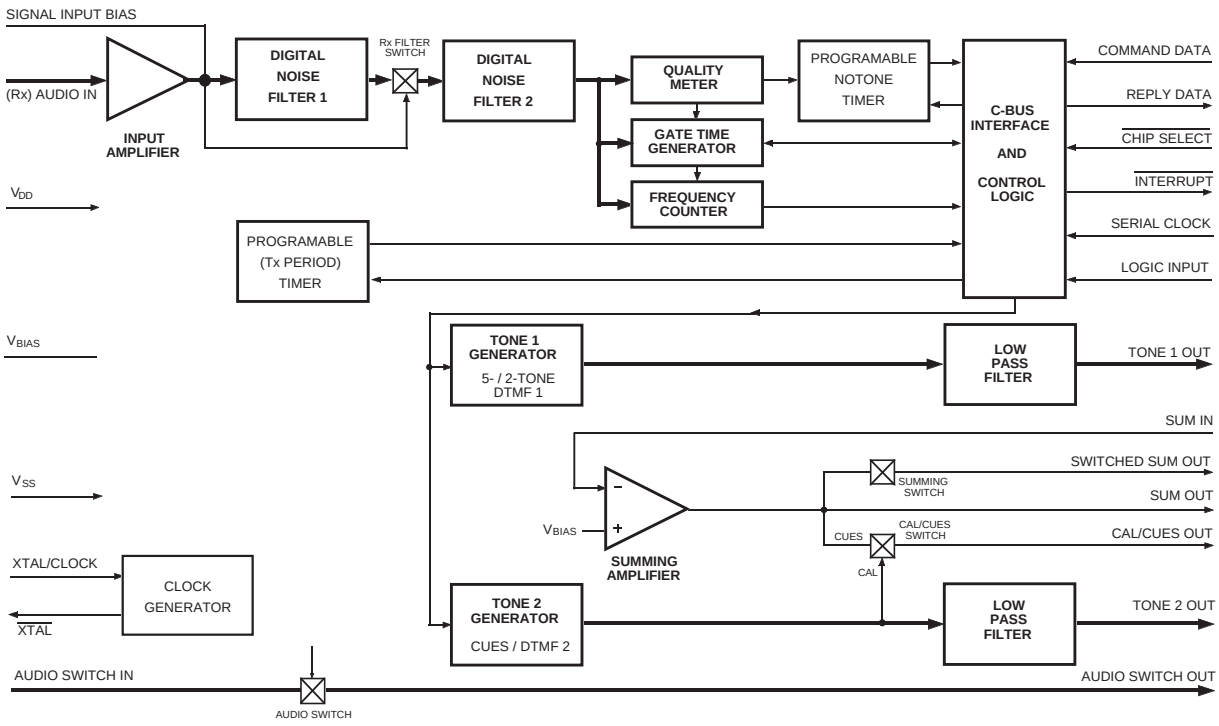


Fig.1 FX803 Audio Signalling Processor

FX803 Audio Signalling Processor

As part of the DBS 800 System, this audio signalling processor will provide an inband tone signalling facility for PMR radio systems. Signalling systems supported include Selcall (CCIR, ZVEI I, II and III, EEA), 2-Tone Selcall and Dual Tone Multi-Frequency (DTMF) encode.

Using a non-predictive tone decoder and versatile encoders gives the FX803 the capability to work in any standard or non-standard tone system.

This is a full-duplex device consisting of:

- Two individual tone generators and a programmable (Tx) period timer.
- A tone decoder with programmable NOTONE Timer.
- An on-chip summing amplifier.

For use with Single Tone or Selective Call systems.

Under the control of the µController, via “C-BUS,” the FX803 will encode and transmit a single or pair of audio tones, in the frequency range 208Hz to 3kHz, simultaneously, and detect, decode and indicate the frequency of non-predicted input tones in the frequency range 313Hz to 6kHz.

Both tone generators can be individually placed into a power economical “Powersave” mode.

A general purpose logic input, interfacing directly with the Status Register, is provided. This could be used as an auxiliary method of routeing digital information to the µController via the “C-BUS.”

The output frequencies are produced from data loaded to the device, with a programmable, general purpose, on-chip timer available to indicate the tone transmit periods.

A Dual Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This Summing Amplifier output is also available for level adjustment.

Tones produced by the FX803 can also be used in the DBS 800 system as modulation calibration inputs and for “CUE” audio indications for the operator.

Received tones are measured and their frequency indicated to the µController in the form of a received data word. A poor-quality or incoherent tone will, after a programmed period, indicate NOTONE.

The FX803 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

Publication D/803/6 April 1998

Pin Number Function

J/LG/LS	DW	
1	1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2.
2	2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock (f_{XTAL}) should be connected here. See Figure 2.
3	3	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{\text{Chip Select}}$ input. This 3-state output is held at high-impedance when not sending data to the µController. See Timing Diagrams.
4	5	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagram.
5	6	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
6	7	**Logic Input:** This 'real-time' input is available as a general purpose logic input port which can be read from the Status Register. See Table 3.
7	8	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive. The System $\overline{\text{IRQ}}$ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below: G/Purpose Timer Period Expired — NOTONE Timer Period Expired — Rx Tone Measurement Complete These interrupts are inactive during relevant Powersave conditions and can be disabled by Bits 5 and 6 in the Control Register.
8	4	No internal connection, connect to V_{SS}.
9	9	No internal connection, connect to V_{SS}.
10	10	**Audio Switch In:** The input to the stand-alone, on-chip Audio Switch. This switching function (Control Register Bit 7) may be used to break the system transmitter modulation path when it is required to provide a CUE (beep) from Tone Generator 2 to the loudspeaker via the FX806 PLMR Audio Processor.
11	11	**Audio Switch Out:** The output of the stand-alone, on-chip Audio Switch.
12	12	**V_{ss}:** Negative Supply (Signal Ground).

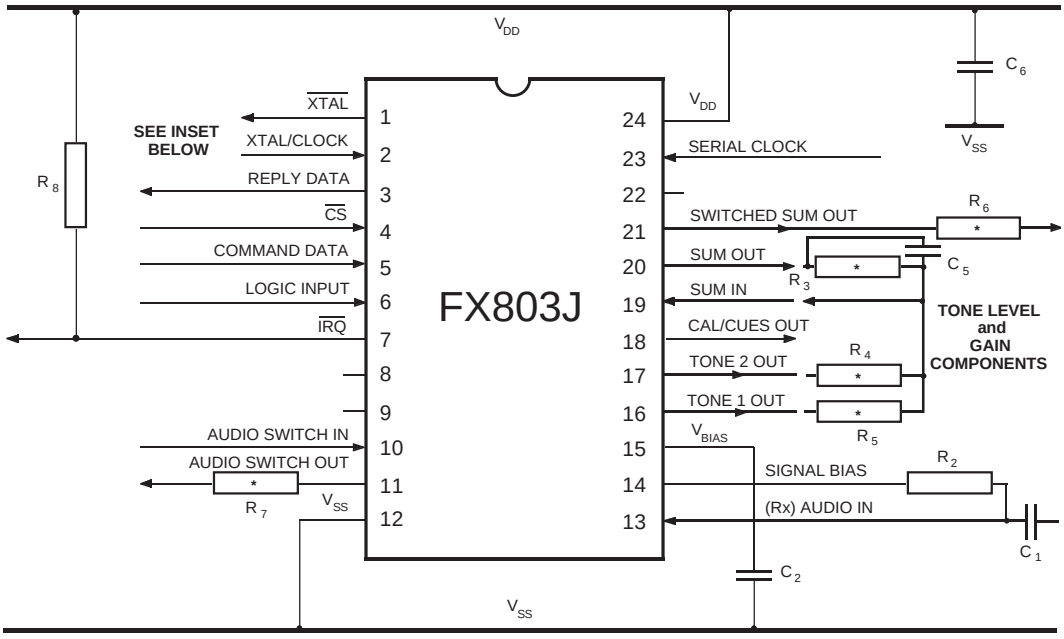
Pin Number Function

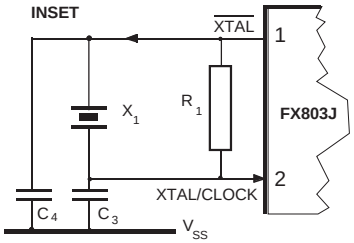
J/LG/LS	DW	
13	13	**(Rx) Audio In:** The received audio tone signalling input to the Input Amplifier. This input requires to be a.c. coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2.
14	14	**Signal Input Bias:** External components are required between this input and the (Rx) Audio In pin See Figure 2.
15	15	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_2 See Figure 2.
16	16	**Tone 1 Out:** Tone 1 Generator (2-/5- tone Selcall or DTMF 1) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 1 Register (Table 4). See Figure 2.
17	17	**Tone 2 Out:** Tone 2 Generator (2-/5- tone Selcall, CUES or DTMF 2) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 2 Register (Table 5). See Figure 2.
18	18	**CAL/CUES Out:** An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the Tx Tone Generator 2 Register (Table 5). In a DBS 800 audio installation, this output should be connected to the Calibration Input of the FX806 PLMR Audio Processor. When Tone Generator 2 is set to V_{BIAS} (NOTONE), the CAL output is pulled to V_{BIAS} and during a powersave of Tone Generator 2 it is held at V_{SS}.
19	19	**Sum In:** The input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figures 2 and 3.
20	20	**Sum Out:** The output of the on-chip Summing Amplifier. Combined tones (1 and 2) are available at this output. See Figures 2 and 3.
21	21	**Switched Sum Out:** The combined tone output available for transmitter modulation. The switch allows control of the FX803 final output to the FX806. Control of this switch is by Bit 4 of the Control Register. See Figures 2 and 3.
22	22	No internal connection, connect to V_{SS}.
23	23	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Audio Signalling Processor. See Timing Diagrams.
24	24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Audio Signalling Processor are dependent upon this supply.

NOTE: (i) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document.

"C-BUS" *is CML's proprietary standard for the transmission of commands and data between a µController and DBS 800 microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*

External Components





Component		Value
R_1	=	1.0MΩ
R_2		2.0MΩ
$*R_3$		100kΩ
$*R_4$		82.0kΩ
$*R_5$		122kΩ
$*R_6$		100kΩ
$*R_7$		100kΩ
R_8		22.0kΩ

C_1	=	0.1µF
C_2		1.0µF
C_3		33.0pF
C_4		33.0pF
C_5		22.0pF
C_6		1.0µF
X_1	f_{XTAL}	4.00MHz

Tolerance: R = ± 10% C = ± 20%

Fig.2 Recommended External Components

Notes

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/1 April 1986. The DBS 800 System Support Document contains additional notes on the use of Xtal/clock frequencies (f_{XTAL}).

2. It is recommended that, to improve screening and reduce noise levels around the FX803, Pins 8, 9 and 22 are connected to V_{SS}.

3. Resistors marked with an asterisk (*) are System Components, calculated to operate in a system with other DBS 800 microcircuits. Figure 3 shows in detail, these components used in the System signal paths.

   R_3, R_4, R_5, C_5 – Tone mixing components to provide a 3dB tone-differential (twist) when used in a DTMF configuration. Single tone output levels are set independently or by the FX806 Modulator Drivers.

   R_7 – Modulation level and matching for inputs to the FX806.

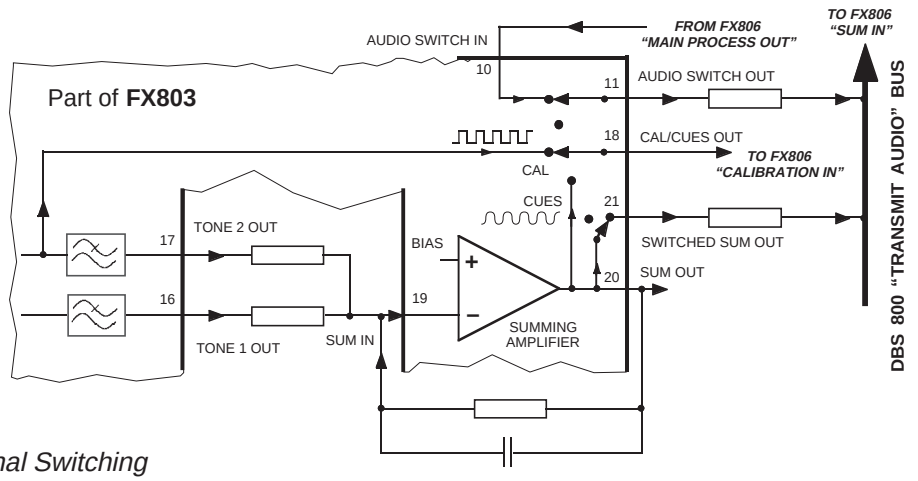


Fig.3 Output Signal Switching

Controlling Protocol

Control of the FX803 Audio Signalling Processor's operation is by communication between the µController and the FX803 internal registers on the “C-BUS,” using Address/Commands (A/Cs) and appended instructions or data (see Figure 7). The use and content of these instructions is detailed in the following paragraphs and tables.

FX803 Internal Registers

FX803 internal registers are detailed below:

Control Register (30_H) – Write Only, control and configuration of the FX803.

Status Register (31_H) – Read Only, reporting of device functions.

Rx Tone Frequency Register (32_H) – Read Only, indicates frequency of the last received input.

Rx NOTONE Timer Register (33_H) – Write Only, setting of the Rx NOTONE period.

Tx Tone Generator 1 Register (34_H) – Write Only, setting the required output frequency from Tx Tone Generator 1.

Tx Tone Generator 2 Register (35_H) – Write Only, setting required output frequency from Tx Tone Generator 2.

General Purpose Timer Register (36_H) – Write Only, setting of a general purpose, sequential time period.

Address/Commands

The first byte of a loaded data sequence is always recognized by the “C-BUS” as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via “C-BUS,” in accordance with the timing information given in Figures 7 and 8.

Table 1 shows the list of A/C bytes relevant to the FX803. A complete list of DBS 800 “C-BUS” Address allocations is published in the System Support Document.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	30	0 0 1 1 0 0 0 0	+	1 byte Instruction to Control Register
Read Status Register	31	0 0 1 1 0 0 0 1	+	1 byte Reply from Status Register
Read Rx Tone Frequency	32	0 0 1 1 0 0 1 0	+	2 byte Reply from Rx Tone Register
Write to NOTONE Timer	33	0 0 1 1 0 0 1 1	+	1 byte Instruction to NOTONE Register
Write to Tx Tone Gen. 1	34	0 0 1 1 0 1 0 0	+	2 byte Instruction to Tx Tone Gen. 1
Write to Tx Tone Gen. 2	35	0 0 1 1 0 1 0 1	+	2 byte Instruction to Tx Tone Gen. 2
Write to G/Purpose Timer	36	0 0 1 1 0 1 1 0	+	1 byte Instruction to G/Purpose Timer

Table 1 “C-BUS” Address/Commands

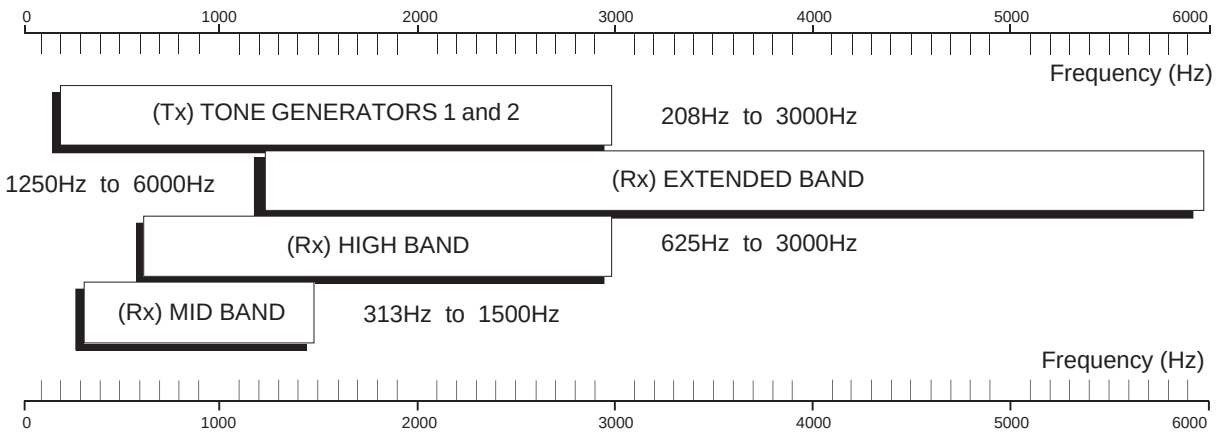


Fig.4 FX803 Frequencies

Controlling Protocol .....

"Write to Control Register" – A/C 30_H, followed by 1 byte of Command Data.

Audio Switch

See the Signal Switching diagram (Figure 3) and DBS 800 Document for application examples.

General Purpose Timer

Should be set up before interrupts are enabled, as a General Reset command will set the timer period to 00_H – 0ms (permanent interrupt).

Interrupt Enable Instructions

Status Bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection

Bits 2 and 3 set the required frequency range (see Figure 4, FX803 Frequencies).

Summing Switch

To break the FX803 drive to the FX806 PLMR Audio Processor (see Figure 3, Signal Switching).

Interrupt Designation

Decoder Interrupts:
No Tone Timer and Rx Tone Measurement.

Transmitter Interrupt:
G/Purpose Timer Interrupt.

Setting	*Control Bits*
MSB Bit 7	***Transmitted First***
1	**Audio Switch** Enable
0	Disable
6	
1	**G/Purpose Timer Interrupt** Enable
0	Disable
5	
1	**Decoder Interrupts** Enable
0	Disable
4	
1	**Summing Switch** Enable
0	Disable
3 ***2***	
0 0	**Band Selection** High Band
0 1	Mid Band
1 0	Extended Band
1 1	Do Not use this setting
1	
0	Set to "0"
0	
0	Set to "0"

Table 2 Control Register

"Read Status Register" – A/C 31_H, followed by 1 byte of Reply Data.

Reading	*Status Bits*
MSB Bit 7	***Received First***
0	Set to "0"
6	
0	Set to "0"
5	
0	Set to "0"
4	
0	Set to "0"
3	**Logic Input Status**
1	"1"
0	"0"
2	**G/Purpose Timer Period**
1	Expired (IRQ generated if enabled) *(Table 2)*
1	**NOTONE Timer Period**
1	Expired (IRQ generated if enabled) *(Table 2)*
0	**Rx Tone Measurement**
1	Complete (Interrupt Generated)

Table 3 Status Register

Interrupt Requests ($\overline{IRQ}$)

Interrupts on this device are available to draw the attention of the µController to a change in the condition of the bit in the Status Register. However Bits are set in the Status Register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by 'polling' the register.

General Purpose Timer Period

Set to a logic "1" when the timer period has expired.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii New G/Purpose Timer information or,
iii General Reset Command

NOTONE Timer Period

Set to a logic "1" when the timer period has expired.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset Command

Rx Tone Measurement

Set to a logic "1" when the Rx Tone measurement is complete.
Cleared to a logic "0,"

i By a read of the Status Register or,
ii General Reset Command

Controlling Protocol .....

Tx Tone Generator Registers 1 and 2

Each Tx Tone Generator is controlled individually by writing a two-byte command to the relevant Tx Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

"Write to Tx Tone Generator 1 Register" – A/C 34_H followed by 2 bytes of Command Data.

MSB (loaded first)			Bit Numbers												LSB (loaded last)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	"0"	V_{BIAS}/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "**A**." "**A**" is used in the formulas below to set the Tx Tone 1 frequency (f_{TONE} 1).												

The binary number produced by bits 0 to 12 (MSB) is designated "A."
If "A" = all logic "0" then Tx Tone Generator 1 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE).
"0" = Tone 1 Output Enabled.
Bits 14 and 15 (MSB) must be logic "0."

Table 4 Setting Tx Tone Generator 1

"Write to Tx Tone Generator 2 Register" – A/C 35_H followed by 2 bytes of Command Data.

MSB (loaded first)			Bit Numbers												LSB (loaded last)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	CAL/ CUES	V_{BIAS}/ Enable	These 13 bits (0 to 12) are used to produce a binary number, designated "**B**." **"B**" is used in the formulas below to set the Tx Tone 2 frequency (f_{TONE} 2).												

The binary number produced by bits 0 to 12 (MSB) is designated "B."
If "B" = all logic "0" then Tx Tone Generator 2 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at V_{BIAS} (NOTONE).
"0" = Tone 1 Output Enabled.
Bit 14 at logic "1" = Squarewave CAL Output.
"0" = Sinewave CUES Output.
Bit 15 (MSB) must be a logic "0."

Table 5 Setting Tx Tone Generator 2

Notes

(1) Programming Tone Generator 2 to V_{BIAS} (NOTONE) (Bit 13) will place the CAL/CUES Output at V_{BIAS} via a 40kΩ internal resistor.
(2) Programming Tone Generator 2 to Powersave will place the CAL/CUES Output at V_{SS}.
(3) If both Tone Generators (1 and 2) are Powersaved, the Summing Amplifier is also Powersaved.

Calculations

As can be seen from Tables 4 and 5 (above), a binary number ("A" or "B" – Bits 0 to 12) is loaded to the respective Tx Tone Generator. The formulas shown below are used to calculate the required output frequency.

Required Tx Tone output frequency = f_{TONE} 1 or 2
XTAL/clock frequency = f_{XTAL}
Input Data Word (Bits 0 to 12) = "A" or "B"

Formula

$$\mathbf{f_{TONE}}\ (Hz) = \frac{f_{XTAL}\ (Hz)}{4 \times \text{"A" (or "B")}} \qquad \textit{or} \qquad \textbf{Input "A" (or "B")} = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

Tx Tone Frequencies

With reference to Tables 4 and 5 (above), whilst Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters (see "Specification" page).

Controlling Protocol .....

"Read Rx Tone Frequency Register" – A/C 32_H, followed by 2 bytes of Reply Data.

Measurement of Rx Signal Frequency (S_{INPUT})

The measurement details given on Pages 10 and 11 are for a Xtal/clock frequency (f_{XTAL}) of 4.032MHz, a scaling formula for other values of f_{XTAL} is given at the bottom of this page.

The input audio signal (S_{INPUT}) is filtered and measured in the Frequency Counter over a specified "measurement period" (9.125 ms or 18.250 ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit (if enabled) are set.

The Rx Tone Frequency Register will now indicate the signal frequency (S_{INPUT}) in the form of 2 bytes (1 and 0) as illustrated in Figure 6 below.

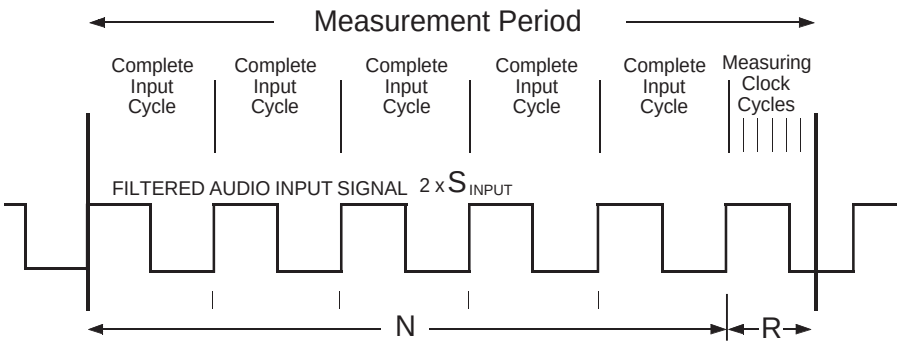


Fig.5 Measurement of a Mid or High Band Rx Frequency

The Integer (N) – Byte 1

A binary number representing *'twice the number of complete input audio cycle periods'* counted during the specified measurement period, which is:

High Band Decode	=	9.125 ms	=	"t"
Mid Band Decode	=	18.250 ms	=	"t"
Extended Band Decode	=	9.125 ms	=	"t"

See the bottom of this page for "t" and "f" scaling factors

The Remainder (R) – Byte 0

A binary number representing the remainder part, R, of 2 x Input Signal Frequency ($S_{INPUT)}$. *'R = number of specified measuring-clock cycles'* required to complete the specified measurement period (See N).

The clock-cycle frequencies are:

High Band Decode	=	56.00 kHz	=	"f"
Mid Band Decode	=	28.00 kHz	=	"f"
Extended Band Decode	=	56.00 kHz	=	"f"

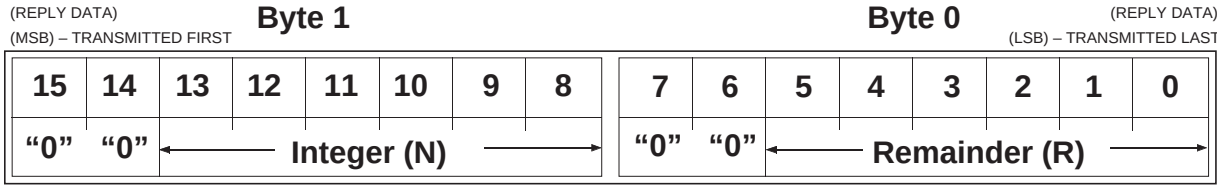


Fig.6 Format of the Rx Tone Frequency Register

f_{XTAL} Scaling Factors

The calculations above are for an f_{XTAL} of 4.032MHz. The following formulas enable the calculation of these values using any Xtal value. Note: f_{XTAL} values are stated in MHz.

$$\text{"t"}_{scaled} = \text{"t"} \times \left[\frac{4.032}{f_{XTAL}} \right]$$

$$\text{"f"}_{scaled} = \text{"f"} \times \left[\frac{f_{XTAL}}{4.032} \right]$$

Controlling Protocol .....

Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured frequency, the following formulæ show the derivation of the Rx frequency, S_{INPUT}, from the measured data bytes (N and R), Figure 6.

High Band Measurement

S_{INPUT} – High Band

In the measurement period of 9.125ms, there are Nh cycles at $2S_{INPUT}$ and Rh clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Nh}{2 \times S_{INPUT}} + \frac{Rh}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{28000 \times Nh}{(511 - Rh)} \text{ Hz} \quad [1]$$

Nh and Rh – High Band

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:

$$2 \times S_{INPUT} \times 9.125 \times 10^{-3} \text{ cycles}$$

Nh is the lower integer value of this decimal number:

$$Nh = \text{INT}(9.125 \times 10^{-3} \times 2 \times S_{INPUT}) \quad [4]$$

Rh is rounded to the nearest integer of this decimal number:

$$Rh = (9.125 \times 10^{-3} - \frac{Nh}{2 \times S_{INPUT}}) \times 56000 \quad [5]$$

Mid Band Measurements

S_{INPUT} – Mid Band

In the measurement period of 18.250ms, there are Nm cycles at $2S_{INPUT}$ and Rm clock cycles at 28.000kHz.

$$\text{so} \quad \frac{Nm}{2 \times S_{INPUT}} + \frac{Rm}{28000} = 18.250\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{14000 \times Nm}{(511 - Rm)} \text{ Hz} \quad [2]$$

N**m** and R**m** – **Mid Band**

The measurement period = 18.250ms
Clock Frequency = 28.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:

$$2 \times S_{INPUT} \times 18.250 \times 10^{-3} \text{ cycles}$$

Nm is the lower integer value of this decimal number:

$$Nm = \text{INT}(18.250 \times 10^{-3} \times 2 \times S_{INPUT}) \quad [6]$$

Rm is rounded to the nearest integer of this decimal number:

$$Rm = (18.250 \times 10^{-3} - \frac{Nm}{2 \times S_{INPUT}}) \times 28000 \quad [7]$$

Extended Band Measurements

S_{INPUT} – Extended Band

In the measurement period of 9.125ms, there are Ne cycles at S_{INPUT} and Re clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Ne}{S_{INPUT}} + \frac{Re}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{56000 \times Ne}{(511 - Re)} \text{ Hz} \quad [3]$$

Ne and Re – Extended Band

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = S_{INPUT} c/s
In the measurement period there are:

$$S_{INPUT} \times 9.125 \times 10^{-3} \text{ cycles}$$

Ne is the lower integer value of this decimal number:

$$Ne = \text{INT}(9.125 \times 10^{-3} \times S_{INPUT}) \quad [8]$$

Re is rounded to the nearest integer of this decimal number:

$$Re = (9.125 \times 10^{-3} - \frac{Ne}{S_{INPUT}}) \times 56000 \quad [9]$$

"Write to the Rx NOTONE Timer Register" – A/C 33_H followed by 1 byte of Command Data.

Setting				*Function/Period*		
MSB						
7	***6***	***5***	***4***	***Transmitted Bit 7 First***		
0	0	0	0	These 4 bits must be "0"		
3	***2***	***1***	***0***	**High/Extended Band**		**Mid Band**
0	0	0	0	period (ms)	0	0
0	0	0	1	"	20 ±1%	40 ±1%
0	0	1	0		40 "	80 "
0	0	1	1		60 "	120 "
0	1	0	0		80 "	160 "
0	1	0	1		100 "	200 "
0	1	1	0		120 "	240 "
0	1	1	1		140 "	280 "
1	0	0	0		160 "	320 "
1	0	0	1		180 "	360 "
1	0	1	0		200 "	400 "
1	0	1	1		220 "	440 "
1	1	0	0		240 "	480 "
1	1	0	1		260 "	520 "
1	1	1	0		280 "	560 "
1	1	1	1		300 "	600 "

Table 6 Rx NOTONE Timer Settings

Operation of the Rx NOTONE Timer

An Rx NOTONE period is that period when no signal or a consistently bad-quality signal is received.

The Rx NOTONE Timer can be employed to indicate to the µController that a NOTONE situation has existed for a predetermined period.

This timer register can be written-to and set in any mode of the FX803.

The NOTONE Timer period is 'primed' by writing to the NOTONE Timer Register (33_H) using the settings given in Table 6.

"Priming" sets the timing period; ***this period can only start directly after a frequency (tone) measurement has been successfully completed.***

The NOTONE Timer is a one-shot timer being reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down.

On completion of the preset period, the NOTONe Timer Period Expired bit in the Status Register and the Interrupt (when enabled, *Table 2*) are set.

Upon detection of the Interrupt, the Status Register should be read by the µController to ascertain the source of the Interrupt.

The NOTONe Timer Period Expired bit is cleared:

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset command

This timer is set to 00_H (0ms) by a General Reset command.

The following situations may be encountered by the NOTONE Timer circuitry:

No Signal

The NOTONE Timer can only start its run down on completion of a valid frequency measurement.

No Signal after a Valid Tone Measurement

The timer will start to run down when the last Rx Tone Measurement complete bit is set. At the end of the "primed" period the NOTONe Timer Period Expired bit in the Status Register and the Interrupt will be set.

Signal Fades after a Valid Tone Measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONe Timer Period Expired bit in the Status Register and the Interrupt will be set.

Signal Appears after the Timer has Started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

"Write to General Purpose Timer Register" – A/C 36_H followed by 1 byte of Command Data.

Setting				*Function/Period*			
MSB							
7	***6***	***5***	***4***	***Transmitted Bit 7 First***			
0	0	0	0	These 4 bits must be "0"			
3	***2***	***1***	***0***	**High/Extended Band**		**Mid Band**	
				Reset Timer and Start Timing			
0	0	0	0	Period of	0		0
0	0	0	1	"	10 ms	±1%	20 ms ±1%
0	0	1	0		20	"	40 "
0	0	1	1		30	"	60 "
0	1	0	0		40	"	80 "
0	1	0	1		50	"	100 "
0	1	1	0		60	"	120 "
0	1	1	1		70	"	140 "
1	0	0	0		80	"	160 "
1	0	0	1		90	"	180 "
1	0	1	0		100	"	200 "
1	0	1	1		110	"	220 "
1	1	0	0		120	"	240 "
1	1	0	1		130	"	260 "
1	1	1	0		140	"	280 "
1	1	1	1		150	"	300 "

Table 7 General Purpose Timer Settings

Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the FX803, can be employed within the DBS 800 system to indicate time-elapsed periods of between 10ms and 150ms in the High/Extended Band, 20ms and 300ms in the Mid Band, to the μController.

Setting of the timer is by loading a single-byte data word via the "C-BUS," as indicated in Table 7 (left), to the FX803 via the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (Bit 2) in the Status Register and the Interrupt (if enabled) are set.

The General Purpose Timer Expired bit is cleared:

i By a read of the Status Register, or
ii New G/P Timer information, or
iii General Reset command.

When the programmed time period has expired, this timer will reset, restart and continue sequencing until;

i New G/P Timer information is written, or
ii A General Reset command.

The General Purpose Timer Expired bit and the Interrupt will remain set until cleared.

This timer is set to 00_H (0ms) by a General Reset command.

Powersave

Various sections of the FX803 can be placed independently into a power economical condition. Table 8 (below) gives a brief summary of the inactive, power-economical states available to the FX803.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	Tx Tone Gen.1 Reg. (34_H)	All bits = "0"	4
Tone Encoder 2	Tx Tone Gen.2 Reg. (35_H)	All bits = "0"	5
Summing Amplifier	This action is automatic when both Tone Encoders are in the powersave condition.		

Table 8 FX803 Powersave Functions

Powersave Conditions

Xtal/Clock and "C-BUS": This circuitry is always active, on all DBS 800 microcircuits, under any powered/powersaved conditions.

Controlling Protocol .....

Interrupt Requests

An Interrupt ($\overline{IRQ}$), when enabled, is provided by the FX803 to indicate the following conditions to the μController.

NOTONE Timer Period Expired	G/Purpose Timer Period Expired	Rx Tone Measurement Complete
Enabled: By Control Register Bit 5.	**Enabled:** By Control Register Bit 6.	**Enabled:** By Control Register Bit 5.
Set: When the preset Notone Flag is set.	**Set:** When the General Purpose Timer has timed out.	**Set:** When an Rx Frequency Measurement has been successfully completed.
Identified: By Status Register Bit 1.	**Identified:** By Status Register Bit 2.	**Identified:** By Status Register Bit 0.
Cleared: By reading the Status Register.	**Cleared:** By reading the Status Register.	**Cleared:** By reading the Status Register.

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status Bits are transferred to the μController via the "C-BUS" Reply Data line and the internal Status Bits are cleared.

Operational Recommendations

It is recommended that, following initial System power-up a General Reset command is sent to the FX803.

Receive Sequence

1. Send Control Command for Rx:
   Select Midband/Highband and Digital Filter length.
2. Disable transmitters, if desired by writing to Tone Frequency registers.
3. Prime the NOTONE Timer by sending the required period byte.
4. Enable Decoder interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt sent to the μC.
6. The μC examines the Status Register, if tone measurement is complete, reads in the Rx Tone Frequency in the form N + R (Figure 6).
7. Rx Tone Measurement Complete interrupts are periodically sent to the μC unless NOTONE is detected, in which case a NOTONE Interrupt is sent.

Transmit Control Sequence

1. Set Tone Frequency Generators to V_{BIAS} (setting both tone generators (Bit 13 = "1")) during the transmitter initialization period.
2. Send Control Command for Tx:
   Select Sum/Switched Sum o/p and Audio Switch states.
3. Send General Purpose (GP) Timer information for the V_{BIAS} (NOTONE) transmitter initialization period (Step 1). This will initiate the timer.
4. Enable the General Purpose Timer interrupt.
5. μC waits for "GP Timer Expired;" Reads the Status Register to check interrupt due to timer; Resets the Status Bit.
   If required, the μC sends the next timer period followed by the next tone(s) frequency information.
   A new timer period sent will reset the timer, otherwise the timer is self-sequencing.
6. The μC monitors the interrupts and repeats 5 & 6 as required.
7. After last loaded tone the μC turns off the Tone Generator(s) by setting tone outputs to V_{BIAS} (NOTONE) (Tables 4 and 5).

General Reset

Upon Power-Up the "bits" in the FX803 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX803.

Control Reg.	Set as 00_H
Status Reg. Bits 0, 1, 2.)	Set as 00_H
NOTONE Timer Reg.	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen/Purpose Reg.	Set as 00_H

Sets the FX803 to:
Encoder High Band (625Hz to 3000Hz) – with interrupts disabled, both timers set to 00_H.

It is recommended that both timers are set-up before interrupts are enabled, to prevent initial, undesired interrupts.

Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

f_{XTAL}	Xtal/clock frequency
S_{INPUT}	Audio input signal
f_{TONE}	Tone frequency

Timing Information

Timing Diagrams

Figure 7 shows the timing parameters for two-way communication between the µController and the FX803 on the “C-BUS.” Figure 8 shows, in detail, the timing relationships for “C-BUS” information transfer.

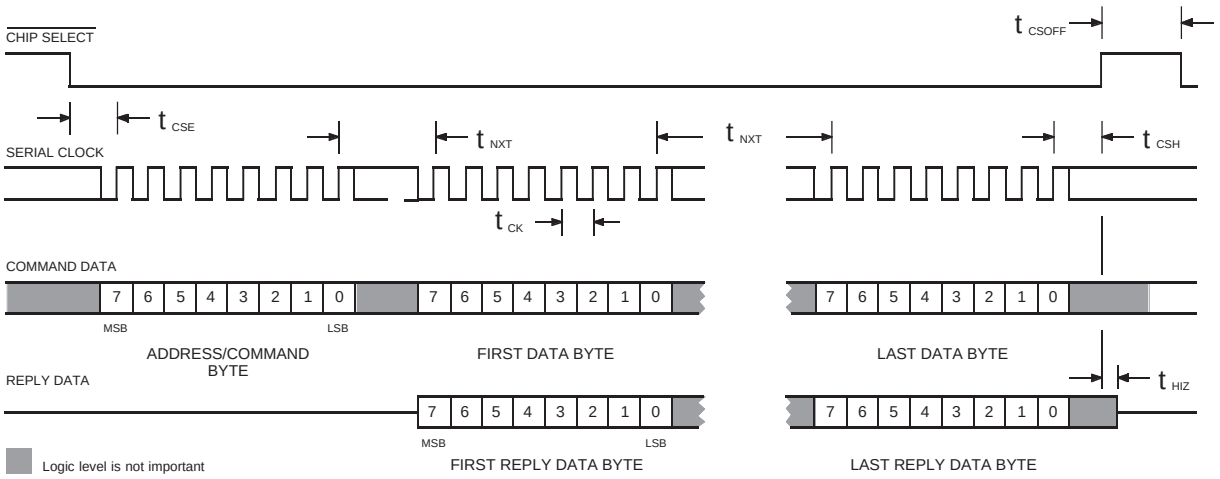


Fig.7 “C-BUS” Timing Information

NOT TO SCALE

Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs
t_{CH}	500	–	–	ns
t_{CL}	500	–	–	ns
t_{CDS}	250	–	–	ns
t_{CDH}	0	–	–	ns
t_{RDS}	250	–	–	ns
t_{RDH}	50.0	–	–	ns
t_{HIZ}	–	–	2.0	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
Reply Data is read from the FX803 MSB (Bit 7) first, LSB (Bit 0) last.
(2) Data is clocked into the FX803 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX803 will work with either polarity Serial Clock pulses.

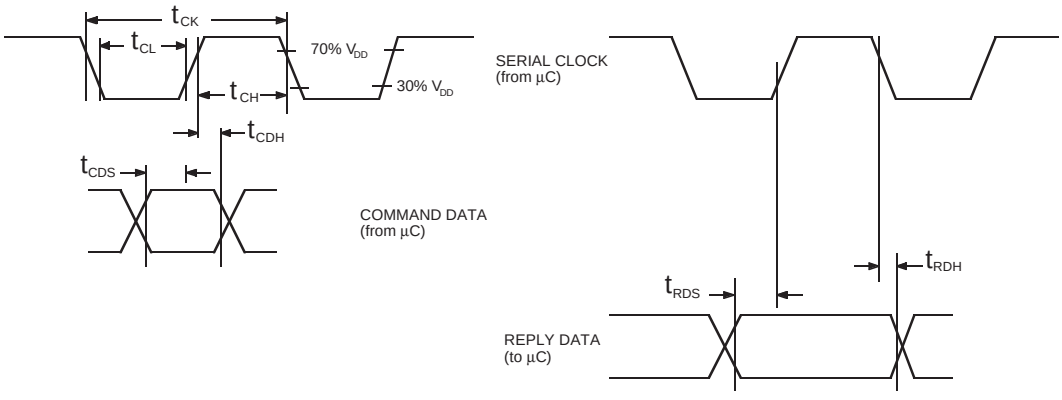


Fig.8 “C-BUS” Timing Relationships

NOT TO SCALE

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX803J**	-40°C to +85°C (cerdip)
	FX803DW/LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX803J**	-55°C to +125°C (cerdip)
	FX803DW/LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock (f_{XTAL}) = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM)*.

Noise Bandwidth = 5.0kHz Band-Limited Gaussian.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
(Decoder + Both Timers)		–	2.0	–	mA
(Decoder + Both Timers + One Tx only)		–	4.0	–	mA
(All Functions Enabled)		–	5.0	–	mA
Analogue Impedances					
(Rx) Audio Input		–	20.0	–	MΩ
Summing Amp Input		–	20.0	–	MΩ
Switch		–	1.0	–	kΩ
Tones 1 and 2 Outputs		–	10.0	–	kΩ
CAL/CUES Output		–	5.0	–	kΩ
Summing Outputs		–	10.0	–	kΩ
Dynamic Values					
Digital Interface					
Input Logic “1”	1	3.5	–	–	V
Input Logic “0”	1	–	–	1.5	V
Output Logic “1” (IOH = -120µA)	2	4.6	–	–	V
Output Logic “0” (IOL = 360µA)	3	–	–	0.4	V
I_{OUT} Tristate (Logic “1” or “0”)	3	–	–	4.0	µA
Input Capacitance	1	–	–	7.5	pF
IOX (V_{OUT} = 5.0V)	4	–	–	4.0	µA
Overall Performance					
Rx – Decoding					
High-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	5	–	–	30.0	ms
Tone-to-Noise Ratio = 0dB	5, 6	–	–	40.0	ms
Frequency					
Band		625		3000	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Rx – Decoding					
Mid-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	7	–	–	60.0	ms
Tone-to-Noise Ratio = 0dB	6, 7	–	–	80.0	ms
Frequency					
Band		313		1500	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%
Extended-Band					
Sensitivity		–	-20.0	–	dB
Tone Response Time					
Good Signal	5	–	–	20.0	ms
Frequency					
Band		1250		6000	Hz
Measurement Resolution		–	0.2	–	%
Measurement Accuracy	9	–	0.5	–	%
Tx – Encoders 1 and 2					
Tone Frequency		208		3000	Hz
Period ($1/f_{TONE}$) Error		–	–	1.0	µs
Tone Amplitude		-1.0	–	1.0	dB
Total Harmonic Distortion		–	–	5.0	%
Rise Time to 90%		–	$3/f_{TONE}$	–	secs
Fall Time to 10%	8	–	–	5.0	ms
Frequency Change Time		–	$3/f_{TONE}$	–	secs
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0		150	ms
Mid-Band		20.0		300	ms
Rx NOTONE					
Timing Period Range					
High-Band		20.0		300	ms
Mid-Band		40.0		600	ms
Xtal/Clock Frequency (f_{XTAL})		3.9	–	6.0	MHz

Notes

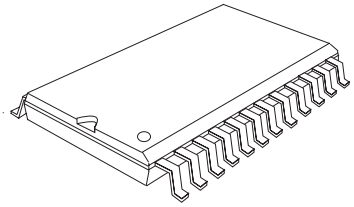
1. Device control pins; Serial Clock, Command Data, and $\overline{CS}$.
2. Reply Data output.
3. Reply Data and $\overline{IRQ}$ outputs.
4. Leakage current into the “Off” $\overline{IRQ}$ output.
5. Measurement Period = 9.125ms.
6. Decode Probability = 0.993.
7. Measurement Period = 18.250ms.
8. When set to Powersave.
9. For a good input signal.
10. The use of the FX803 at Xtal/clock frequencies above 4.0MHz will cause a shift in the overall performance parameters.

Package Outlines

The FX803 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX803DW 24-pin plastic S.O.I.C. (D2)

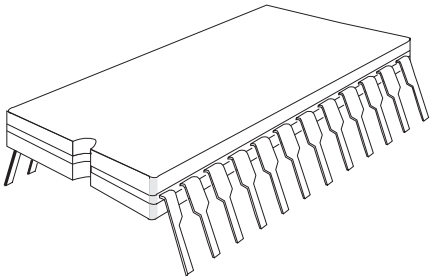
NOT TO SCALE



Max. Body Length 15.57mm
Max. Body Width 7.59mm

FX803J 24-pin cerdip DIL (J4)

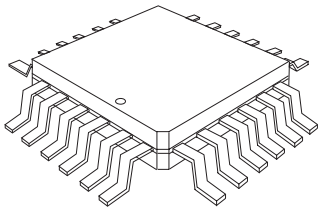
NOT TO SCALE



Max. Body Length 32.00mm
Max. Body Width 13.36mm

FX803LG 24-pin quad plastic encapsulated bent and cropped (L1)

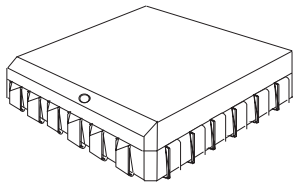
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX803LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Handling Precautions

The FX803 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX803DW 24 pin plastic S.O.I.C. (D2)
FX803J 24-pin cerdip DIL (J4)
FX803LG 24-pin encapsulated bent and cropped (L1)
FX803LS 24-lead plastic leaded chip carrier (L2)